TITLE

DUAL CHIPS STACKED PACKAGING STRUCTURE

BACKGROUND OF THE INVENTION

Field of the Invention

The present invention relates to a semiconductor packaging structure and in particular to a dual chips stacked semiconductor packaging structure.

Description of the Related Art

In recent years, packaging has become a performance-limiting factor for microelectronic devices, with size, weight, cost, pin count, and power consumption assuming importance in packaging design. Packaging design must generally trade off between material, structure, and electronic property considerations to obtain a cost-effective and reliable design.

Conventional stacked semiconductor packaging structure, as shown in Fig. 1, one side of a chip paddle 2 of a lead frame is usually attached to the non-active surface of the first chip 1, with the opposite side attached to the of the second chip 3 by using the epoxy or other adhesive. Wires 5 connect with the leads 4 and the bonding pads 6 deposited on the first chip 1 and the second chip 2. The resulting structure is then encapsulated by a molding compound 7, thus completing the package. It is difficult to integrate the first chip 1 and the second chip into the packaging structure since the active surfaces of the fist chip and the second chip

are opposite each other. Moreover, the total thickness of the stacked packaging structure is thick.

Another conventional stacked semiconductor packaging structure is shown in Fig. 2. A spacer 30 is disposed between the first chip 100 and the second chip 20. The active surfaces of the first chip 10 and the second chip 20 face the same direction. However, the total thickness of the stacked semiconductor packaging structure as mentioned above is still overly thick. Furthermore, the stacked semiconductor packaging structure is asymmetrical, affecting reliability.

SUMMARY OF THE INVENTION

Accordingly, an object of the invention is to provide a dual chips stacked packaging structure to assemble two chips facing the same direction, compatible with the current products, to simplify packaging and reduce costs.

It is another object of the invention to provide a dual chips stacked packaging structure with reduced total thickness.

To achieve the above objects, the present invention provides a dual chips stacked packaging structure comprising a first chip, a lead frame, a second chip, and a plurality of wires. The first chip comprises an active surface and an opposing non-active surface, the active surface consisting of a central area and a peripheral area having a plurality of first bonding pads. The lead frame comprises a plurality of leads and a chip paddle having a first adhering surface and a second adhering

surface, wherein the first adhering surface is adhered to the active surface of the first chip in such a way as to avoid contact with the first bonding pads. A second chip comprises an active surface and an opposing non-active surface connecting with the second adhering surface of the chip paddle, wherein the active surface consists of a central area and a peripheral area having a plurality of second bonding pads. As well, parts of the wires electrically connect with the first bonding pad and the leads, and parts of the wires electrically connect with the second bonding pad and the leads.

The first adhering surface of the chip paddle and the active surface of the first chip are connected by a non-conductive solid or liquid adhesive.

The second adhering surface of the chip paddle and the non-active surface of the second chip are connected by a solid or liquid adhesive. Further, the wires can be metal.

Each lead has a connecting surface and non-connecting surface.

The structure of further comprises an encapsulation, covering the lead frame, the first chip, the second chip, the wires, and the non-connecting surface of each lead.

The arrangement of the encapsulation can be modified in several ways.

In one modification, the encapsulation covers the second chip, the chip paddle, the connecting surface of each lead, the wires, and the active surface of the first chip, exposing the opposing non-active surface of the first chip and the non-connecting surface of each lead.

Each lead further comprises an inner lead covered by the encapsulation and outer lead extending beyond the encapsulation.

A detailed description is given in the following embodiments with reference to the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

The present invention can be more fully understood by reading the subsequent detailed description and examples with references made to the accompanying drawings, wherein:

FIG. 1 is a cross-section of a conventional stacked semiconductor packaging structure;

FIG. 2 is a cross-section of another conventional stacked semiconductor packaging structure;

FIG. 3 is a cross-section of a dual chips stacked packaging structure according to a first embodiment of the invention;

FIG. 4 is a top-view of the first level of the dual chips stacked packaging structure of Fig. 3;

FIG. 5 is a top-view of the second level of the dual chips stacked packaging structure of Fig. 3;

FIG. 6 is a cross-section of a dual chips stacked packaging structure according to a second embodiment of the invention, wherein the structure comprises an encapsulation;

FIG. 7 is a cross-section of a dual chips stacked packaging structure according to a third embodiment of the invention, wherein the wire non-connecting surfaces of leads are entirely covered by the encapsulation;

FIG. 8 is a cross-section of a dual chips stacked packaging structure according to the third embodiment of the invention, wherein the outer leads extend outside the encapsulation.

DETAILED DESCRIPTION OF THE INVENTION

The present invention is now described with reference to the figures.

First embodiment

In Fig. 3, a dual chips stacked packaging structure according to the present invention is shown. A first chip 100 comprises an active surface 100a and an opposing non-active surface 100b, the active surface 100a consisting of a central area and a peripheral area, on which a plurality of first bonding pads 120a is arranged.

A lead frame comprises a plurality of leads 400 and a chip paddle 300 having a first adhering surface 300a and a second adhering surface 300b. The first adhering surface 300a of the chip paddle 300 is adhered to the active surface 100a of the first chip 100 in such a way as to avoid contact with the first bonding pads 120a, as shown in Fig. 4.

The structure of Fig. 3 can be divided into two levels. The first level comprises the first chip 100, the chip paddle 300, and the leads 400 without the second chip 200, as shown in Fig. 4. The second level comprises the second chip 200, as shown in Fig. 5.

A plurality of leads 400 respectively corresponding to the bonding pads 120a, 120b are individually arranged beside the first chip 100 and the second chip 200. Each

of the leads comprises a wire non-connecting surface II and a wire connecting surface I to connect with wires 140.

A second chip 200 comprises an active surface 200a and an opposing non-active surface 200b connecting with the second adhering surface 300b of the chip paddle 300. The active surface 200a of the second chip 200 consists of a central area and a peripheral area having a plurality of second bonding pads 120b. In particular, both the active surface 100a, 200a of the first chip 100 and the second chip 200 face the same direction.

Parts of the wires 140 electrically connect with the first bonding pad 120a and the leads 400, and parts of wires 140 electrically connect with the second bonding pad 120b and the leads 400. Moreover, the loop height of wires 140 between first bonding pads 120a and the leads 400 are lower than the top surface of the chip paddle 300, such that the wires 140 connecting with the first chip 100 cannot reach the second chip 200.

Second embodiment

The dual chips stacked packaging structure of the present invention as described above can further be covered by an encapsulation to prevent machine or moisture damage. The encapsulation can cover the structure in several ways, described hereafter.

In Fig. 6, an encapsulation 106 covers several elements of the semiconductor packaging structure described in the first embodiment, which, for brevity, is not illustrated here again. In the present embodiment, the first chip 100, the second chip 200, the chip paddle

300, the bonding pad 120, the wires 140, and the leads 400 are covered by the encapsulation 500. The leads can be totally covered by the encapsulation 500 and also extend beyond the encapsulation 500. The parts of the leads 400 covered by the encapsulation 106 are defined as inner leads 400a, and those extending beyond the encapsulation 106 as outer leads 400b.

Third embodiment

In Figs. 7 and 8, the encapsulation 500 covers the dual chips stacked packaging structure described in the first embodiment, which, for brevity, is not illustrated here again.

In the present embodiment, the non-active surface 100b of the first chip 100 and the wire non-connecting surface of the leads 400 are exposed outside the encapsulation 500. The encapsulation 500 covers only the active surface 100a of the first chip 100, the second chip 200, the chip paddle 300, the bonding pad, and the wire connecting surface of the leads 400. Exposure of the non-connecting surface and the non-active surface further enhances heat dissipation.

The leads 400 can be completely covered by the encapsulation 500, as shown in Fig. 7, and also comprise the inner leads 400a covered by the encapsulation 500 and the outer leads 400b extending beyond the encapsulation 500, as shown in Fig. 8. The outer leads 400b are beneficial for second level packaging.

Accordingly, the present invention provides several advantages. First, the back of the chip (non-active surface) is exposed beyond the encapsulation to improve

heat dissipation, enhancing reliability. Second, compared with the conventional structure, the total thickness of the semiconductor packaging structure of the present invention is significantly reduced, benefiting packaging processes. Third, both the active surface of the first chip and the second chip face the same direction, such that the first bonding pads and the second pads can be formed by the same design without different chips. Fourth, the dual chips stacked packaging structure is symmetrical, effectively improving reliability.

While the invention has been described by way of example and in terms of the preferred embodiments, it is to be understood that the invention is not limited to the disclosed embodiments. To the contrary, it is intended to cover various modifications and similar arrangements (as would be apparent to those skilled in the art). Therefore, the scope of the appended claims should be accorded the broadest interpretation to encompass all such modifications and similar arrangements.